862.2400 D2

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	:	Examiner: N.Y.A.
ATSUSHI DATE ET AL.	)	
	:	Group Art Unit: N.Y.A.
Appln. No.: Divisional of Appl. 09/122,012, filed July 24, 1998	)	
	:	
	)	
Filed: Concurrently Herewith	:	
	)	
For: BUS MANAGER AND CONTROL APPARATUS FOR MULTIFUNCTION DEVICE HAVING SAID BUS MANAGER	:	
	)	July 30, 2001

Commissioner for Patents
BOX PATENT APPLICATION
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the Title to read:

--BUS MANAGEMENT BASED ON BUS STATUS--.

IN THE SPECIFICATION:

At page 1, immediately after the Title, insert:

--CROSS REFERENCE TO RELATED APPLICATION

This application is a division of Application No. 09/122,012, filed July 24, 1998, now allowed.--.

Please substitute the paragraph starting at page 19, line 6 and ending at page 19, line 25 with the following replacement paragraph (a version of this paragraph, marked to show changes, is appended):

--Fig. 4 is a block diagram of the DoEngine. The DoEngine, indicated at 400, was designed and developed as a controller mainly of next-generation multifunction peripherals (MFPs) or multifunction systems (MFSs). A MIPS R400 core manufactured by MIPS Technologies, Inc. is employed as a CPU (processor core) 401. Packaged in the processor core 401 are cache memories of 8 KB each for instructions and data, and MMU, etc. The processor core 401 is connected to a system bus bridge (SBB) 402 via a 64-bit processor bus (P-bus). The SBB 402 is a 4 x 4 64-bit crossbar switch and is also connected to a memory controller 403, which is for controlling an SDRAM and ROM and has a cache memory, via a special-purpose local bus (MC bus), and to a G bus 404, which is a graphics bus, and an IO bus 405, which is an input/output bus. Thus, the system bus bridge 402 is connected to a total of four buses. The system bus bridge 402 is connected to these buses on a one-to-one basis. To the greatest extent possible the system bus bridge 402 is designed in such a manner that the two pairs of buses can be connected in parallel.--

Please substitute the paragraph starting at page 37, line 12 and ending at page 37, line 19 with the following replacement paragraph (a version of this paragraph, marked to show changes, is appended):

--The SBB 402 is a multichannel bidirectional bus bridge which provides the interconnection among the IO bus (input/output), G bus (graphics bus), P bus (processor local bus) and MC bus by using a crossbar switch. By virtue of the crossbar switch, the connections of two systems can be established simultaneously and it is possible to realize high-speed data transfer with a high degree of parallel operation.--

Please substitute the paragraph starting at page 64, line 23 and ending at page 64, line 26 with the following replacement paragraph (a version of this paragraph, marked to show changes, is appended):

--The type of arbitration is decided by the present bus switch connection state and a priority set in advance. The result is a changeover in the address switch and data switch connections.--

IN THE CLAIMS

Please cancel Claims 1-16 without prejudice or disclaimer of the subject matter recited therein.

REMARKS AND CLAIM TO PRIORITY

This is a divisional application of Application No. 09/122,012, filed July 24, 1998 ("the '012 Application").

Claims 17-20 are pending in this application. Claim 17 is independent.

The specification has been amended to include reference to the '012 Application, and to make the changes made in that application.

Applicants claim priority under 35 U.S.C. § 119 based upon Japanese Priority Application No. 9-200570, filed July 25, 1997, and respectfully request acknowledgment of this claim and of receipt of the certified copy of the priority document, which was filed September 30, 1998, in the '012 Application.

An Information Disclosure Statement is submitted herewith.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

Attorney for Applicants

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VERSION TO SHOW CHANGES MADE TO SPECIFICATION

The title has been amended as follows:

[BUS MANAGER AND CONTROL APPARATUS FOR MULTIFUNCTION DEVICE HAVING SAID BUS MANAGER] BUS MANAGEMENT BASED ON BUS STATUS.

At page 1, immediately after the Title, the following section has been added:

--CROSS REFERENCE TO RELATED APPLICATION

This application is a division of Application No. 09/122,012, filed July 24, 1998, now allowed.--.

The paragraph starting at page 19, line 6 and ending at page 19, line 25 has been amended as follows:

Fig. 4 is a block diagram of the DoEngine. The DoEngine, indicated at 400, was designed and developed as a controller mainly of next-generation multifunction peripherals (MFPs) or multifunction systems (MFSs). A MIPS R400 core manufactured by MIPS Technologies, Inc. is employed as a CPU (processor core) 401. Packaged in the processor core 401 are cache memories of 8 KB each for instructions and data, and MMU, etc. The processor core 401 is connected to a system bus bridge (SBB) 402 via a 64-bit processor bus (P-bus). The SBB 402 is a 4 x 4 64-bit [cross-bus] crossbar switch and is also connected to a memory controller 403, which is for controlling an [SDREAM]

SDRAM and ROM and has a cache memory, via a special-purpose local bus (MC bus), and to a G bus 404, which is a graphics bus, and an IO bus 405, which is an input/output bus. Thus, the system bus bridge 402 is connected to a total of four buses. The system bus bridge 402 is connected to these buses on a one-to-one basis. To the greatest extent possible the system bus bridge 402 is designed in such a manner that the two pairs of buses can be connected in parallel.

The paragraph starting at page 37, line 12 and ending at page 37, line 19 has been amended s follows:

The SBB 402 is a multichannel bidirectional bus bridge which provides the interconnection among the IO bus (input/output), G bus (graphics bus), P bus (processor local bus) and MC bus by using a [cross-bus] crossbar switch. By virtue of the [cross-bus] crossbar switch, the connections of two systems can be established simultaneously and it is possible to realize high-speed data transfer with a high degree of parallel operation.

The paragraph starting at page 64, line 23 and ending at page 64, line 26 has been amended as follows:

The type of arbitration is decided by the present bus switch connection state and a [prior] priority set in advance. The result is a changeover in the address switch and data switch connections.